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In the claims:

All of the claims standing for examination are reproduced below with appropriate status indication.

1-31. (Canceled)

32. (Currently amended) A semiconductor package assembly, comprising:

a die having electrical contact pads for external connection and a height; [[and]]
a predominantly metal substrate having a recessed area with a depth at least equal to the height of the die; and
solder balls between the electrical contact pads of the die and patterned circuitry on the substrate in the recessed area thereby mounting the die to the substrate and connecting to the substrate circuitry;

wherein the substrate comprises a dielectric layer on the recessed side insulating the patterned circuitry extending into the recessed area, the die is mounted in the recessed area with electrical connections provided between the electrical contact pads of the die and the patterned circuitry in the recessed area, vias are formed through the dielectric layer separating the metal substrate from the patterned circuitry, and a plurality of solder ball connections are made to the metal of the substrate from individual ones of the contact pads of the die, providing direct, conductive heat transfer between the die and the metal of the substrate.

33. (Canceled)

34. (Currently amended) The semiconductor package assembly of claim [[33]]32 further comprising solder balls mounted to individual traces of the substrate patterned circuitry in area outside the recessed area providing facility to connect the traces to circuitry on a

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printed circuit board.

35. (Canceled)

36. (Previously presented) The semiconductor package assembly of claim 32 wherein the metal of the predominantly metal substrate is predominantly copper or stainless steel.

37. (Previously presented) The semiconductor package assembly of claim 32 wherein the die is mounted to the substrate in the recessed area by adhesive with the electrical contact pads facing away from the substrate, and the electrical connections are provided between the electrical contact pads of the die and the patterned circuitry in the recessed area by wire bonds.

38. (Previously presented) The semiconductor package assembly of claim 37 further comprising plastic material encapsulating the die and the wire bonds, and either package pins or solder balls connected to individual traces of the substrate patterned circuitry in substrate area outside the recessed area.

39-45. (Canceled)

46. (Currently amended) A substrate for a semiconductor package, comprising:
a metal plate having a central recessed area;
a dielectric layer formed on the metal plate on the recessed side;
patterned, electrically-conductive circuitry formed on the dielectric layer,
electrically insulated from the metal plate, the circuitry extending into the recessed area
and vias formed through the dielectric layer, providing direct, heat-conducting paths from the circuitry side of the substrate to the metal plate.

47. (Canceled)

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48. (Previously presented) The substrate of claim 46 further comprising either contact pins or solder balls mounted to the patterned, electrically-conductive circuitry in the area outside the recessed area

49-51. (Canceled)